PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

YOSHIHIKO TOYODA

Application No.: Unknown

Art Unit: Unknown

Examiner: Unknown

Filed: June 28, 2001

For: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A semiconductor device comprising:

an insulating layer having a surface and including a plurality of grooves having different widths; and

a conductive layer filling each of the grooves and including at least a plated layer, wherein a bottom portion of some of the grooves is non-planar.

2. The semiconductor device according to claim 1, wherein the non-planar bottom portions have a ratio of depth to width of not more than 0.7.

3. The semiconductor device according to claim 1, wherein the non-planar bottom portions have a ratio of depth to width of not more than 0.35.

4. The semiconductor device according to claim 1, wherein the non-planar bottom portions include a concave portion having a groove shape, with a ratio of depth to width greater than 0.35.

5. The semiconductor device according to claim 1, wherein the non-planar bottom portions include a concave portion having a groove shape, with a ratio of depth to width greater than 0.7.

6. The semiconductor device according to claim 1, wherein the non-planar bottom portion includes a concave portion having a hole shape, with a ratio of depth to width greater than
0.35.

7. The semiconductor device according to claim 1, wherein the non-planar bottom portion includes a concave portion having a hole shape, with a ratio of the depth to the width of greater than
0.7.

8. The semiconductor device according to claim 1, wherein the non-planar bottom portion has a concave portion having two slanting side faces intersecting each other in a cross-sectional view.

9. The semiconductor device according to claim 8, wherein the side faces are slanted with an angle greater than 20 degrees relative to the surface of said insulating layer.

10. The semiconductor device according to claim 1, wherein the non-planar bottom portions of the grooves have concave portions with a pitch not more than 4 times width of the concave portions.

11. A manufacturing method of a semiconductor device comprising:

forming a plurality of grooves having different widths on a surface of an insulating layer, and forming non-planar bottom surfaces in some of the plurality of grooves;

plating a metal film on said insulating layer and embedded in the plurality of grooves on the non-planar bottom portions; and

removing said metal film by chemical mechanical polishing until at least the surface of said insulating layer is exposed so that said metal film remains in the grooves and on the non-planar bottom portions as an interconnection layer.

12. The manufacturing method of a semiconductor device according to claim 11, further comprising:

forming a lower interconnection layer beneath said insulating layer; and

forming a connection hole for connecting said lower interconnection layer and said interconnection layer in said insulating layer, prior to forming the grooves, and simultaneously forming the connection hole and said non-planar portions.